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3.5 Gb/s x 4 ch Optical Interconnection Module for ATM Switching System

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Abstract

The developed optical interconnection module contains an AlN ceramic package with low thermal resistance, an LSI chip integrating the 3.5-Gb/s, 4-ch transmitter or receiver, and an optical submodule, which is assembled using a new passive-alignment technique. The use of the LSI chip reduces size to 6.5 cc and power dissipation to 6.1 W. The time needed to assemble the optical submodule is decreased to 1/20 by using the passive-alignment technique.

Introduction

Asynchronous-transfer-mode (ATM) switching systems with a throughput of more than 1 Tbit/s are required for future broadband integrated services digital networks (B-ISDNs). Advances in very large-scale integrated circuit technology will provide the switching devices needed to meet this requirement. The interconnections between such devices on different printed circuit boards will be bottlenecks to high-speed data transfer due to their limited signal bandwidth and limited number of input-output connections. Optical interconnection modules for board-to-board and rack-to-rack interconnections will eliminate these bottlenecks, resulting in high-capacity, high-speed switching systems [1].

We have developed a 3.5-Gb/s, 4-ch optical interconnection module for high-throughput board-to-board interconnections. This module (Fig. 1) consists of an AlN multilayer ceramic package, a 3.5-Gb/s, 4-ch parallel optical interconnection LSI chip [2], and a parallel optical submodule for E/O or O/E conversion. The size is 40×20 mm^2; the power dissipation is 2.5 W for the transmitter module and 3.6 W for the receiver module. The size and power dissipation are decreased drastically by using the LSI chip [3]. A new passive-alignment technique using microcapillaries between the four-channel LD array and a hemispherically lensed-multimode fiber array reduces the alignment time to less than 1/20 that of conventional active alignment. Because of the small foot print of the optical interconnection module, four pairs of the transmitter and receiver modules can be mounted on an ATM switching board [4]. Throughput of an ATM switching board is thus increased four times.

Module structure

Figure 2 shows a cross-section and bottom view of the module which consists of an electrical submodule and an optical submodule. The electrical submodule consists of an AlN ceramic multilayer package, a transmitter (TX) or receiver (RX) LSI, and chip capacitors. The package has two cavities for mounting an LSI and an optical submodule. The LSI is mounted on the cavity and wired to the pads on the package. The chip bypass capacitors are also mounted for an RX module.

The optical submodule contains Si substrate with V-grooves, either a LD or PD array,

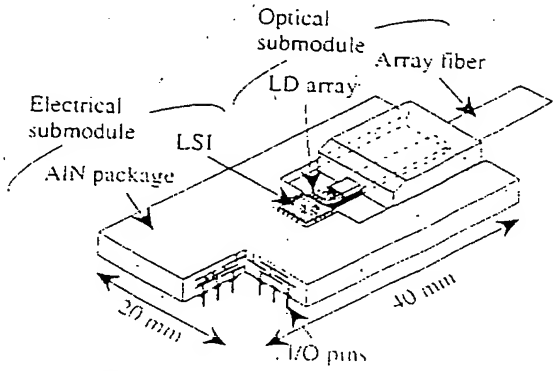

Fig. 1. Optical interconnection module structure.

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microcapillaries, and a fiber array. The LD or PD array is mounted on the Si substrate. Microcapillaries are fixed into the V-grooves. The microcapillaries enable the passive alignment between the LD or PD array and the fiber array. The electrical and optical submodules are assembled and tested independently. After testing, the optical submodule is mounted on the electrical submodule and wired to the LSI chip. Finally, a metal cap and fins are assembled on the module.

In the following section, key technologies for our optical interconnection module are described including the design of LSI chips, package design, and passive-alignment technique.

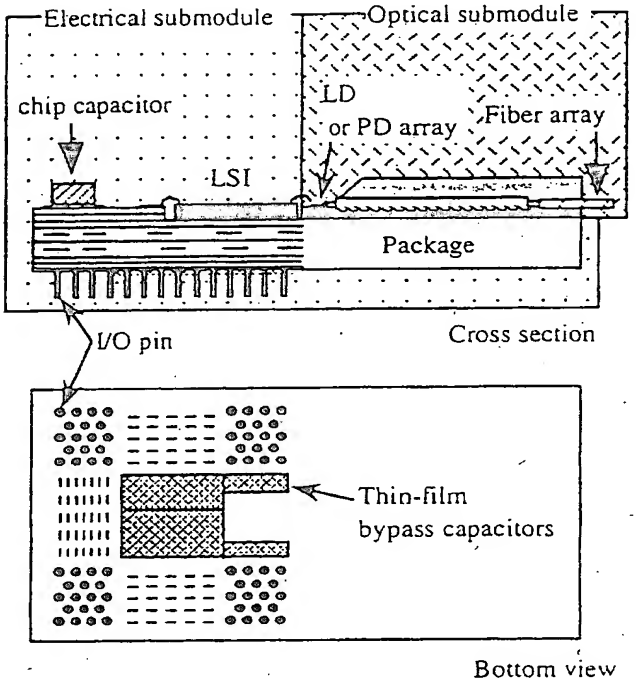

Fig.2. Cross section and bottom view of interconnection module.

Design of LSI chips

To reduces the module size and power dissipation, we have developed the four channel parallel optical interconnection LSI chips which contains all electrical circuits required for optical interconnection. Figure 3 shows a block diagram of the TX and RX LSI chip.

Each channel of the TX chip has a 5-to-1 multiplexer (MUX), a phase locked loop (PLL) circuit for generating a 3.5-GHz internal clock signal for the MUX, and an LD driver. The electrical inputs are five 700-Mb/s lines for data and a pair of 700-MHz differential clocks. The input signals for each channel are encoded with modified 4B1C coding and multiplexed into 3.5-Gb/s signals synchronized with the 700-MHz input clock signal [2]. This reduces the maximum number of consecutive 0s or 1s to less than 10. The receiver circuit thus does not have to handle long sequence of 0s or 1s resulting in stable operation.

Each channel of the RX chip contains an amplifier, an automatic offset canceling circuit (AOC), a data and clock recovery PLL circuit, and a 1-to-5 demultiplexer with a frame synchronization circuit. The electrical outputs are five 700-Mb/s lines for data and a pair of 700-MHz differential clocks. The demultiplexer circuit synchronizes the frames to ensure that the parallel data are output in the correct order.

The TX and RX LSI chips are fabricated using a 0.5-μm Si-bipolar process; their power dissipations are respectively 2.5 W and 3.6 W.

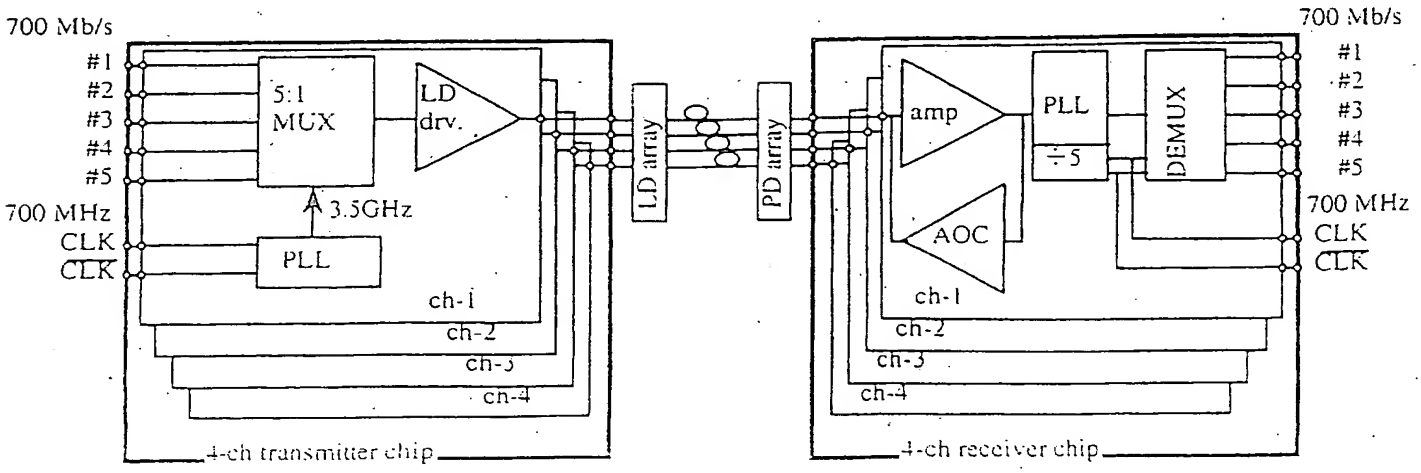

Fig. 3. Block diagram of 4-ch TX and RX LSI chips

Package design

Because the electrical signal is very high speed, cross-talk between signal lines is a serious problem in miniaturization. Furthermore, cooling of the module is also a serious concern. Consequently, we use AlN ceramic, which has low thermal resistance, as the material for this package substrate. The characteristic impedances of the signal lines are controlled to reduce the signal reflection.

The signal lines on the surface of the package are microstrip lines with 50-Ω characteristic impedance. These lines are placed with a 150-μm pitch to match the LSI chip pad pitch. The cross-talk between lines is calculated to determine their maximum permissible length. Figure 4 shows the calculated cross-talk. The near-end cross-talk is less than -20 dB for 3-mm parallel lengths. The other signal lines in the internal layers are strip lines with 50-Ω characteristic impedance and a minimum pitch of 300-μm. Figure 5 shows the calculated cross-talk for the strip lines. Their near-end cross-talk is less than -20 dB for 5-mm parallel lengths. This package has 11 metal layers including the surface. Three layers are used as signal layers, and the other layers are used for power supply.

Because our RX LSI chip integrates four amplifiers, the electrical noise of their power supplies must be reduced. We did this by forming thin-film bypass capacitors on the bottom of the package. Additionally, the receiver module contains chip capacitors as additional bypass capacitors.

The thermal resistance of this package for various air velocities was calculated to determine the cooling conditions. Figure 6 shows a cross-section of the simulation model. The calculated package had a metal cap and fins, and the assumed power dissipation of the LSI chip was 4 watts. Figure 7 shows the simulated and measured thermal resistances. The thermal resistance becomes small enough at an air velocity more than 1 m/s.

This package has butt-lead PGA structure for I/O pins to reduce the space required for mounting on a board. Ground or power pins are placed around signal pins to reduce cross-talk between signal pins.

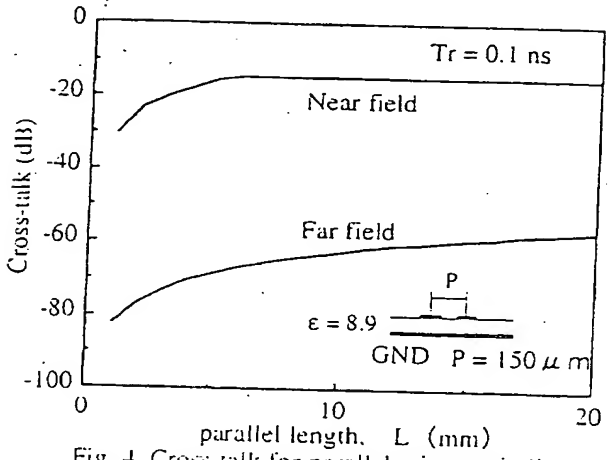

Fig. 4. Cross-talk for parallel micro-strip lines.

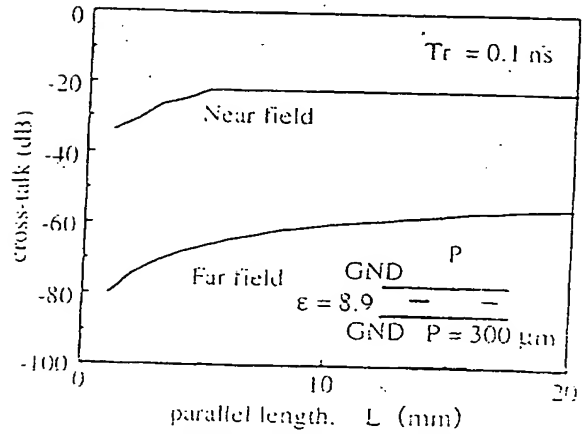

Fig. 5. Cross-talk for parallel strip lines.

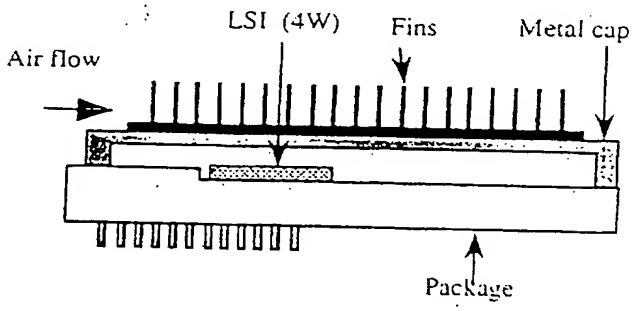

Fig. 6. Thermal simulation model.

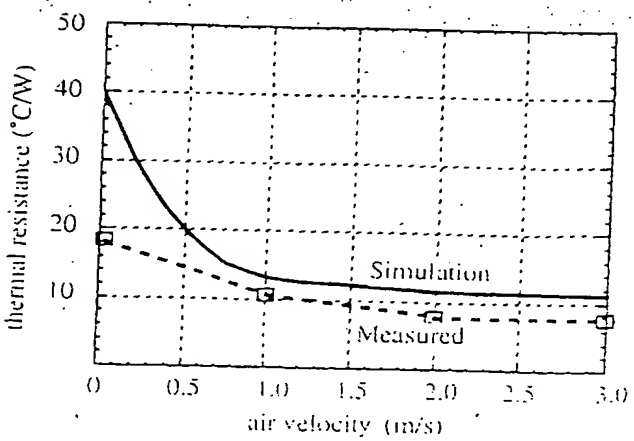

Fig. 7. Thermal resistance from chip to air.

Passive-alignment technique

In the conventional parallel optical interconnection module, the LD array on the substrate is coupled by actively aligning the arrayed hemispherically lensed-fiber component. This requires a complicated, time-consuming process for controlling the six degrees of freedom individually. To reduce the assembly cost, we have developed a technique for passively aligning the LD array with the hemispherically lensed-multimode fiber array by using microcapillaries. Figure 8 shows the optical coupling structure. The 250-μm-pitched four-channel LD array is bonded to a thin solder pattern on a Si platform. A thin stop layer to prevent the melted solder from spreading over the ground layer effectively controls the rotation of the LD array during die bonding. The fiber array is composed of hemispherically lensed-multimode fibers (GI-50/125 μm) with a radius of 50-μm for high-efficiency coupling [3]. The normalized coupling tolerances of the actively aligned lensed fiber to the LD are shown in Fig. 9. Alignment errors at a coupling-loss fluctuation of 0.5 dB are obtained within a wide range (±4 μm) in the x and y directions and from -3 to 9 μm in the z direction. These wide tolerances enable mechanical assembly of the coupling structure without using an alignment device. The microcapillaries, which have an inner diameter of 126 μm for fiber-guiding, are the key parts to passively aligning the fiber array. The alignment in the angular and x directions is done passively by fixing the capillaries in 250-μm-pitched Si V-grooves. The outer diameter of each capillary has an accuracy of better than 1 μm, so LD-fiber alignment in the y direction is precisely controlled by selecting a suitable outer diameter for the capillary, as shown Fig. 10. The height h, of the capillary center above the platform surface is determined from the half-width of the V-groove a, and the radius of the capillary L:

$$h = (L^2 - a^2)^{1/2} .$$

The height can be varied within a range of 20 μm by setting 2L between 224 and 248 μm. This means that fluctuations in the emitting height of LD arrays can be compensated for by selecting a suitable outer diameter. As a result, alignment control is only needed in the z direction. This alignment is easily done by sliding the fiber array through the capillaries till they reach the stair-shaped positioning marker, which has a 10μm

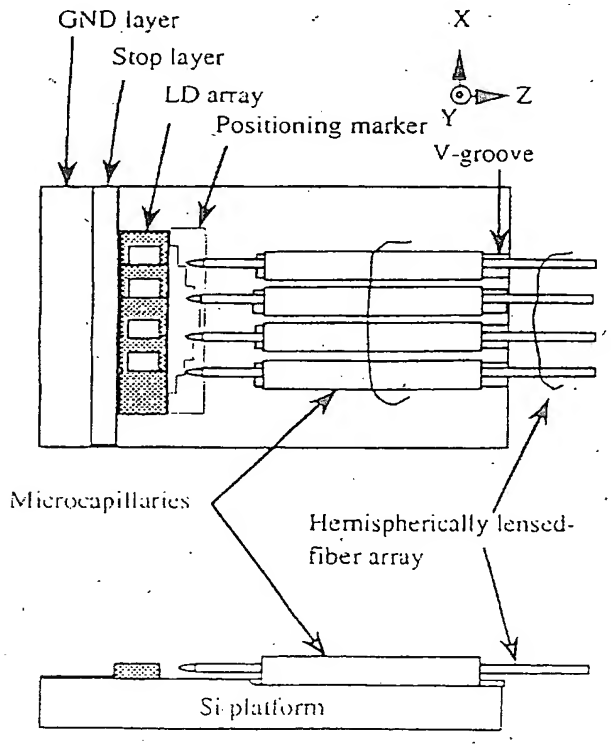

Fig. 8. Optical coupling structure using microcapillaries.

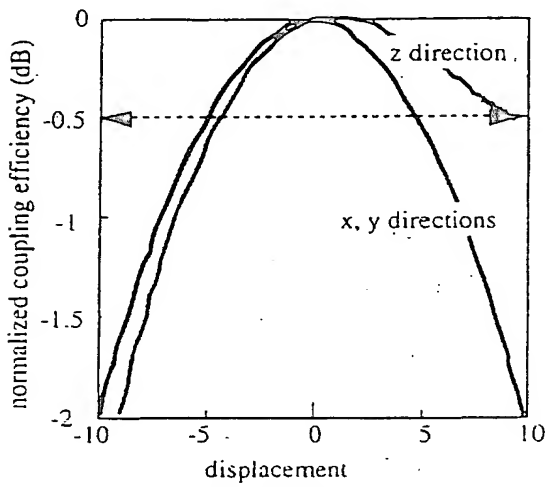

Fig. 9. Coupling tolerances between hemispherically lensed fiber and LD.

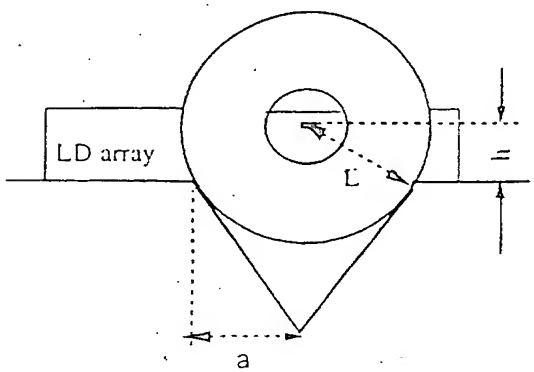

Fig. 10. Suitable outer diameter of capillary.

step, because of the wide coupling tolerance in the z direction. Figure 11 shows a photograph of the coupling. The alignment time was reduced to less than 1/20 that of conventional active alignment [3]. The coupled light-current characteristics of this coupling structure are shown in Fig. 12, along with those of the detected optical power for an uncoupled-LD array. A coupling efficiency of -3.0 dB, which is equal to that of a conventional active-aligned submodule [3], was obtained within a ±0.5 dB deviation among the channels at a bias of 10 mA.

The optical coupling between the PD array and fiber array is shown in Fig. 13. The substrate of the PD array has two floors. The array is mounted on the lower floor of the substrate, and 250-μm-pitched V-grooves for the micro-capillary are formed on the upper floor. The alignment in the angular and x directions is passively done by fixing the capillaries in the grooves. Another substrate with 250-μm-pitched V-grooves is used to place the fiber array at a 250-μm pitch. The fiber array is inserted into microcapillaries on the V-grooves; its fiber ends are then slant-polished. The coupling efficiency is 0.4 dB ±0.1 dB using 35° slanted fibers. A photograph of the optical coupling between the slant-polished fiber array and the PD array is shown in Fig. 14.

Figure 15 shows a photograph of both modules without cap and fins.

Module test

Because the electrical I/O signal is very fast, we used a new testing socket that can transmit high speed signals to measure the module characteristics. Figure 16 shows a cross section of the testing socket, which consists of a socket base, a module holder, and a press plate. The socket base consists of a metal base, action pins for electrical I/O, two guide pins for the module holder and press plate, and two press handles. Each I/O pin has a coaxial structure to transmit high-speed electrical signals. Cylindrical insulators are inserted in the metal base and the action pins are placed in the center of each insulator. The metal base

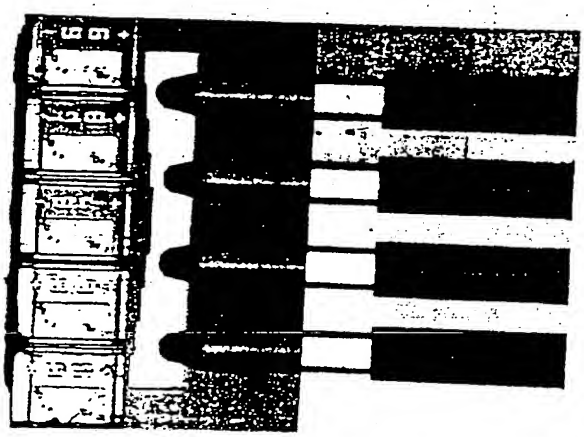

Fig. 11. Photograph of coupling between LD and fiber array.

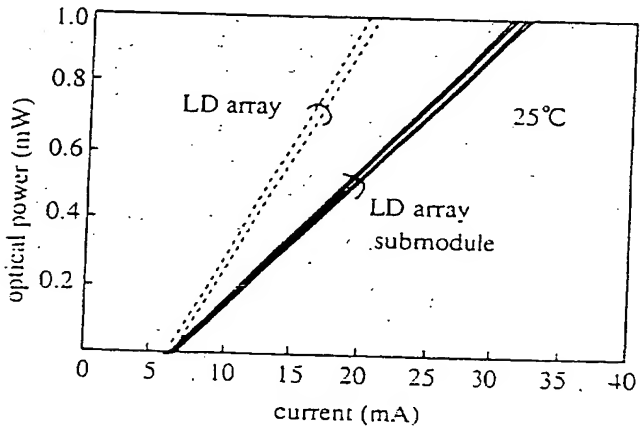

Fig. 12. Coupled light-current characteristics.

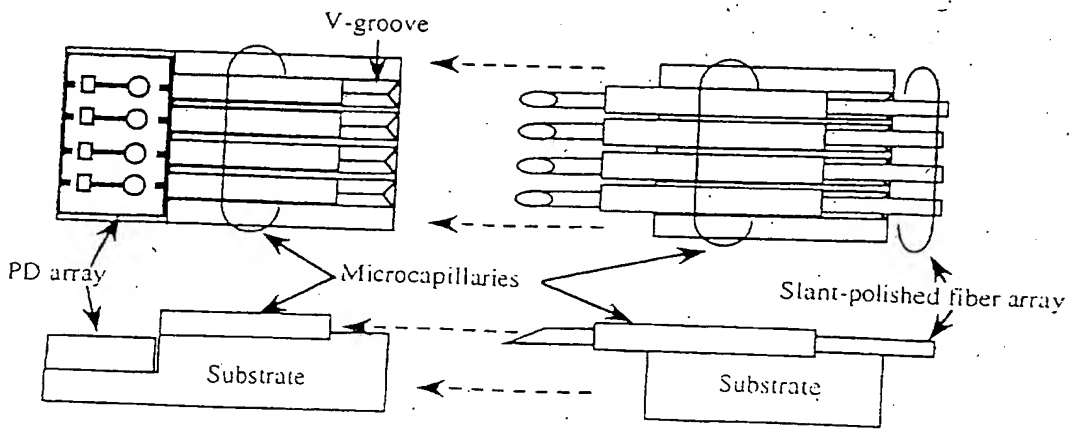

Fig. 13. Optical coupling between PD array and fiber array.

works as shield for the coaxial structures, and, the action pins are the center conductors. The characteristic impedance of the coaxial structures are 50 Ω. The module holder holds either a TX or RX module; it is used to align each signal pin to an action pin on the base by using the guide pins. Through holes are formed in the bottom plate of the module holder. All I/O pins of the module are inserted in these holes and fixed to the action pins. Hooking the press handle of the base to the press plate presses the module against the base.

The experimental optical output waveform of the TX module when all four channels were active is shown in Fig. 17. A 3.5-Gb/s data stream was correctly output for each channel. The output waveform of the RX electrical submodule when all for channels were active is shown in Fig. 18. The data was regenerated correctly.

Summary

A 3.5-Gb/s, 4-ch parallel optical interconnection module for ATM switching system has been developed. It has either a TX or a RX LSI chip integrating the optical interconnection circuits. The volume of the module is only 6.5 cc which is 1/10 of conventional one with the same throughput, the power dissipation is also reduced to 1/4. Moreover, the alignment time for the optical submodule is reduced to less than 1/20 that of conventional active alignment by using a new passive-alignment technique with microcapillaries.

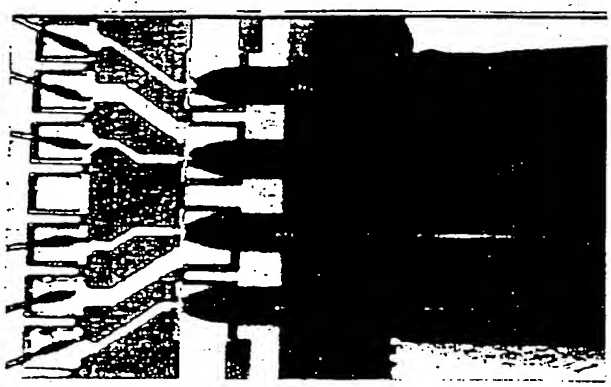

Fig. 14. Photograph of optical coupling.

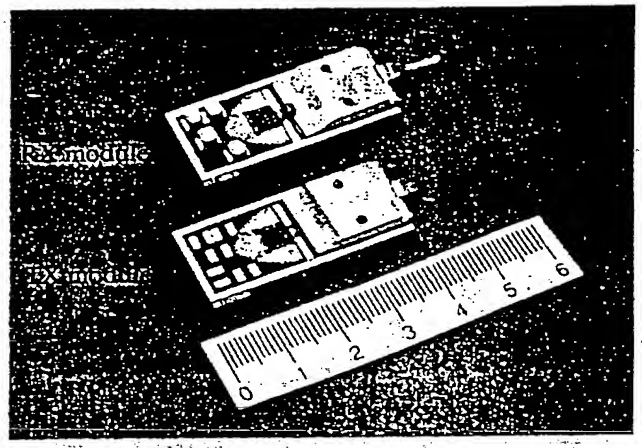

Fig. 15. Photograph of optical interconnection module.

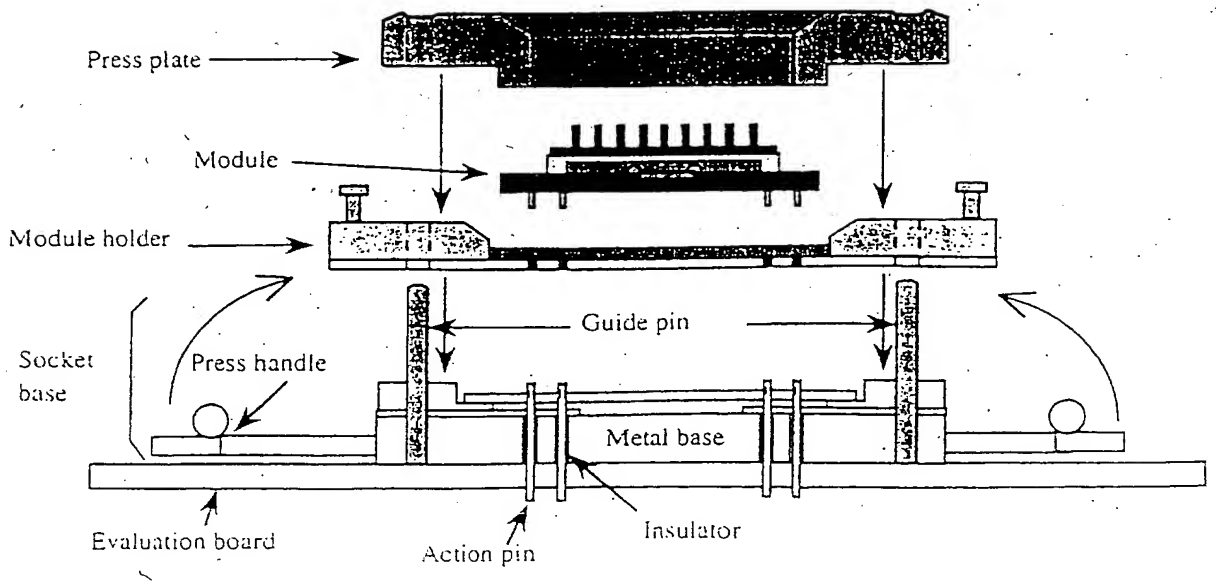

Fig. 16. Cross section of testing socket.

Acknowledgment

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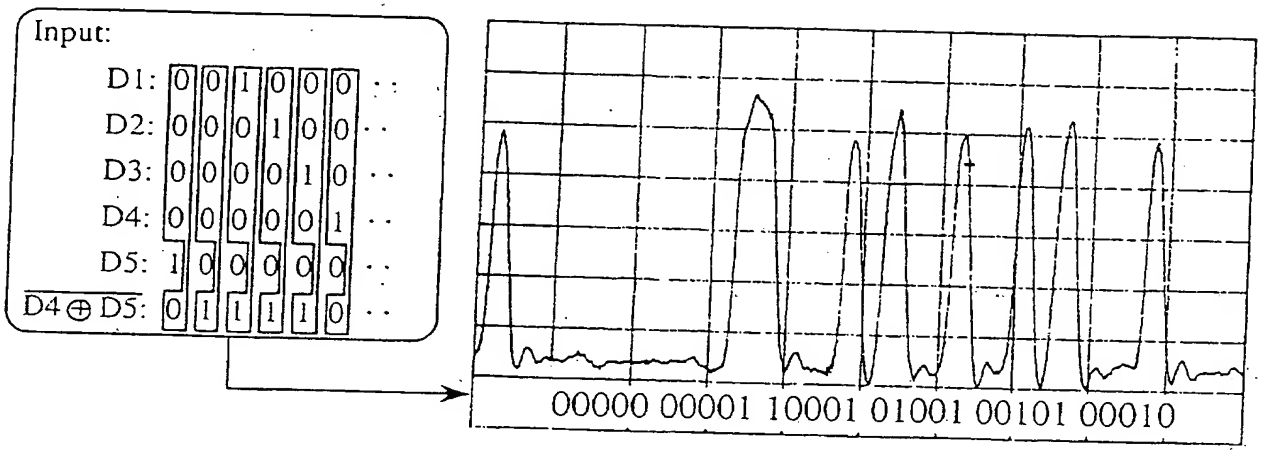

Fig. 17. Optical output waveform of TX module.

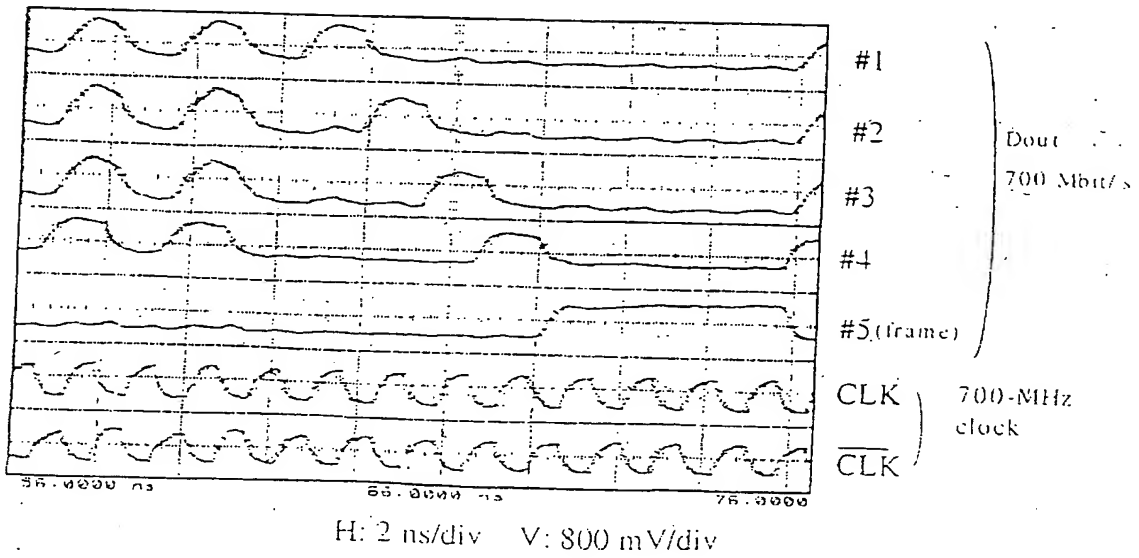

Fig. 18. Output waveform of RX electrical submodule.